AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions, and listings, of claims in the captioned patent application:

Listing of Claims:

1. (Currently Amended) A margin testing system for frequency margin testing an electronic system, the margin testing system comprising:

a baseboard management controller;

an ~~I^2C I/O expander~~ Inter-Integrated Circuit I/O expander configured to generate bit patterns in response to commands from said baseboard management controller; and

a digital frequency synthesizer connected to ~~the I^2C I/O expander~~ said Inter-Integrated Circuit I/O expander by an ~~I^2C I/O bus~~ Inter-Integrated Circuit I/O bus and configured to generate one or more test frequencies for application to one or more of a plurality of components of said electronic system in response to bit patterns generated by ~~the I^2C I/O expander~~ said Inter-Integrated Circuit I/O expander;

wherein said baseboard management controller is configured to monitor a response ~~of the~~ of said plurality of components of said electronic system to said one or more test frequencies, and

wherein ~~the plurality~~ said plurality of components are operably connected within said electronic system such that no invasive connection is necessary to ~~apply the~~ apply said one or more test frequencies.

2. (Currently Amended) The margin testing system of claim 1, wherein said ~~claim 1 wherein the~~ baseboard management controller, in monitoring said response ~~the response~~ of said electronic system, is further configured to collect and analyze data regarding a response of one or more selected components of said system to said test frequencies.

3. (Canceled)

4. (Currently Amended) The margin testing system of claim 1, further comprising:

a hardware monitor configured to communicate with said baseboard management controller and said frequency synthesizer to measure values of said one or more test frequencies and to transmit said measured values to said controller.

5. (Previously Presented) The margin testing system of claim 4, wherein said hardware monitor is further configured to communicate with selected ones of said components to receive data regarding response of said components to said one or more test frequencies.

6. (Currently Amended) The margin testing system of claim 1, wherein said controller is further configured to transmit command signals to said frequency synthesizer to ~~cause the~~ cause said synthesizer to generate said one or more test frequencies.

7. (Canceled)

8. (Currently Amended) The margin testing system of claim 1, wherein ~~said BMC~~ said baseboard management controller implements Intelligent Platform Management Interface (IPMI) protocol.

9. (Currently Amended) The margin testing system of claim 1, further comprising:

an ~~I^2C-based bus~~ Inter-Integrated Circuit-based bus for providing communication between ~~said BMC~~ said baseboard management controller and said frequency synthesizer.

10. (Currently Amended) The margin testing system of claim 9, wherein said ~~I^2C-based bus~~ Inter-Integrated Circuit-based bus comprises:

an IPMB bus.

11. (Currently Amended) The margin testing system of claim 1, wherein said frequency synthesizer receives an input reference clock signal, and in response to a command signal from said baseboard management controller, generates an output clock signal as a multiple of said reference clock signal.

12. (Original) The margin testing system of claim 11, wherein said frequency synthesizer applies said output clock signal as a test frequency to said one or more components for frequency margin testing thereof.

13. (Currently Amended) The margin testing system of claim 1, wherein said frequency synthesizer generates each one of a plurality of test frequencies based on a pattern of input bits received ~~from the~~ from said baseboard management controller.

14. (Currently Amended) The margin testing system of claim 1, wherein said baseboard management controller initiates margin testing in response to commands from an external system.

15. (Currently Amended) The margin testing system of claim 14, wherein said external system comprises:

a console in communication with said baseboard management controller via a serial bus.

16. (Currently Amended) The margin testing system of claim 14, wherein said external system comprises:

a remote computer in communication with said baseboard management controller.

17. (Currently Amended) The margin testing system of claim 16, wherein said remote computer communicates with said baseboard management controller via a network-based connection.

18. (Currently Amended) The margin testing system of claim 14, wherein said external system includes a scripting entity for generating commands for transmission to said baseboard management controller.

19. (Original) The margin testing system of claim 1, wherein said one or more components receive nominal clock frequencies in the absence of said test frequencies.

20. (Currently Amended) A computer system, comprising:

a processor;

a plurality of components in communication with said processor for performing a plurality of tasks;

a baseboard management controller;

an ~~I²C I/O expander~~ Inter-Integrated Circuit I/O expander configured to generate bit patterns in response to commands from said baseboard management controller; and

a digital frequency synthesizer connected to ~~the I²C I/O expander~~ said Inter-Integrated Circuit I/O expander by an ~~I²C I/O bus~~ Inter-Integrated Circuit I/O bus and configured to generate one or more test frequencies for application to one or more of a plurality of components of said electronic system in response to bit patterns generated by ~~the I²C I/O expander~~ said Inter-Integrated Circuit I/O expander,

wherein said baseboard management controller is configured to monitor a response of said plurality of components of said computer system to said one or more test frequencies, and

wherein ~~the plurality~~ said plurality of components are operably connected within said computer system such that no invasive connection is necessary to ~~apply the~~ apply said one or more test frequencies.

21. (Canceled)

22. (Currently Amended) The computer system of claim 20, wherein ~~said BMC~~ said baseboard management controller implements an IPMI protocol.

23. (Currently Amended) The computer system of claim 20, further comprising:

an ~~I²C-based bus~~ Inter-Integrated Circuit-based bus for providing communication between ~~said BMC~~ said baseboard management controller and said frequency synthesizer.

24. (Original) The computer system of claim 20, wherein said computer system is a server.

25. (Currently amended) A method for frequency margin testing of one or more components of a computer system, comprising a baseboard management controller, an ~~I^2C I/O expander~~ Inter-Integrated Circuit I/O expander and a digital frequency synthesizer, in communication with said baseboard management controller through an ~~I^2C bus~~ Inter-Integrated Circuit bus and ~~the I^2C I/O expander~~ said Inter-Integrated Circuit I/O expander, comprising:

transmitting, ~~by the~~ by said baseband management controller, one or more commands to said ~~I^2C I/O expander~~ Inter-Integrated Circuit I/O expander and said synthesizer for said frequency margin testing;

generating, by ~~the I^2C I/O expander~~ said Inter-Integrated Circuit I/O expander, bit patterns of input signals ~~to the~~ to said synthesizer ~~from the~~ from said one or more commands;

generating, ~~by the~~ by said synthesizer, one or more test frequencies in response ~~to the~~ to said input signals and for application to said one or more components;

monitoring, ~~by the~~ by said baseband management controller, a response of said one or more of components of said computer system to said test frequencies; and

storing the response as a test result;

wherein ~~the one or more of~~ said one or more components are operably connected within said computer system such that no invasive connection is necessary to apply ~~the one~~ said one or more test frequencies.

26. (Currently Amended) The method of claim 25, wherein monitoring, ~~by the~~ by said baseboard management controller a response ~~of the~~ of said system to each of said test frequencies further comprises:

collecting data regarding a response of one or more selected components of said system to said test frequencies; and

analyzing said collected data.

27. (Previously Presented) The method of claim 25, wherein said baseband management controller implements an intelligent platform management interface (IPMI) protocol.

28. (Currently Amended) The method of claim 27, wherein transmitting, ~~by the~~ by said baseband management controller one or more commands to said synthesizer, comprises:

transmitting said commands over an I^2C ~~-based~~ Inter-Integrated Circuit-based bus.

29. (Currently Amended) The method of claim 25, wherein the step of causing the controller to transmit commands ~~to the~~ to said synthesizer comprises:

transmitting a bit pattern from said controller to said frequency synthesizer to set an output of said synthesizer to a selected value based on said bit pattern.

30. (Currently Amended) The method of claim 25, wherein the method further comprises:

transmitting, ~~by the~~ by said baseband management controller, one or more further commands to said synthesizer for said frequency margin testing of the same component of said one or more components when the stored test result is a failed test result.

31. (Currently Amended) The method of claim 25, wherein the method further comprises:

transmitting, ~~by the~~ by said baseband management controller, one or more further commands to said synthesizer for said frequency margin testing of another component of said one or more component when the stored test result is a successful test result.